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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/873,016	05/30/2001	Chaitanya Palusa	ALNC-9400	3233

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EXAMINER	
TRAN, KHANH C	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 11/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/873,016	PALUSA ET AL.	
	Examiner	Art Unit	
	Khanh Tran	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 May 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 14* is/are rejected.

7)☒ Claim(s) *2-13 and 15-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim is objected to because of the following informalities: in lines 2-3, "the delayed clock signal" should be changed to -- a delayed clock signal --. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. U.S. Patent 6,208,183 B1 in view of Watanabe U.S. Patent 5,910,741.

Regarding claims 1 and 14, figure 3 illustrated a gated delay-locked loop (GDLL) 200 according to Li et al. invention. The GDLL 200 includes:

A voltage-controlled delay 222, including M delay elements (column 8, lines 35-65), varying a timing of an intermediate clocked signal CLK_{D1} in response to a voltage V_{LF};

A phase/frequency detector 202, connected to the voltage-controlled delay 222, detecting a phase difference between a reference clock CLK_{REF} and a delayed CLK_{OUT}. In column 7, lines 23-42, the phase/frequency detector 202 asserting an "UP" signal

when a reference clock signal leads the output delayed clock signal, and asserting an "DOWN" signal when a reference clock signal lags the output delayed clock signal. The phase/frequency detector 202 differs from the claimed phase detector in that the phase/frequency detector 202 asserting no synch signal when the reference clock signal and the output delayed clock signal are in phase. However, by not asserting the "UP" signal and the "DOWN" signal, the phase/frequency detector 202 implies a synch signal. Nevertheless, in column 4 lines 50-67, Watanabe shows a phase comparator 11 in a phase locked loop, wherein the phase comparator 11 generates an up-down signal when a reference clock signal RCLK is phase-advanced to an output clock signal CLK and vice versa, and *a phase lock signal HOLD* when phases of reference clock signal RCLK and output clock signal CLK are in phase. In light of Watanabe teachings, it would have been obvious for one of ordinary skill in the art at the time the invention was made that the phase/frequency detector 202 can be modified to assert a phase lock signal HOLD as taught by Watanabe. The motivation for combining the teachings is that physically asserting the phase lock signal HOLD is evidently a selection at design. The phase/frequency detector 202 as taught by Li et al. still generates three states UP, DOWN, and without any signal for SYNCH, and performs the same function as the claimed phase detector;

In column 7, lines 43-57, a charge pump 204 connected to the phase/frequency detector 202 that outputs a current I_{CP} in response to the output signal from the phase/frequency detector 202. The charge pump 204 produces current I_{CP} instead of a voltage as claimed in the instant application. Nevertheless, a person of average skill in

the art knows that the charge pump 204 can be easily modified to produce a voltage instead;

In column 7, lines 43-57, a loop filter 206, connected between the charge pump 204 and a voltage-controlled delay 222, filters and generates a control voltage V_{LF};

In column 7 line 58 through column 8 line 35, a combination of gating pulse 212, fixed delay 214, MUX 216, flip-flop 218, and voltage-controlled delay 220 varies a timing of the intermediate clock CLK_{D1} with respect to the reference clock CLK_{REF} by adding or subtracting increment units of delay through voltage-controlled delay 220 in response to the control voltage V_{LF}, and the logic states of "UP" "DOWN" and "HOLD" through the output clock CLK_{D1}. In light of the foregoing, the combination performs function as the claimed delay circuit that varies a timing of the intermediate clock signal.

Allowable Subject Matter

3. Claims 2-13 and 15-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Yoshimura et al. U.S. Patent 5,994,934 discloses "Delay Locked Loop Circuit".

McDonagh U.S. Patent 6,239,634 discloses "Apparatus and Method For Ensuring The Correct Start-Up and Locking of a Delay Locked Loop".

Mnich U.S. Patent 6,346,839 discloses "Low Power Consumption Integrated Circuit Delay Locked Loop and Method For Controlling The Same".

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 571-272-3007. The examiner can normally be reached on Monday - Friday from 08:00 AM - 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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